Filter Design HDL Coder Release Notes

These release notes describe the Version 1.0 release of the Filter Design HDL Coder. Topics include

- "Introduction to the Filter Design HDL Coder" on page 2-2
- "Known Software and Documentation Problems" on page 2-4

Printing the Release Notes

To print the Release Notes, link to the PDF version.



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These release notes provide the following information:

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Introduction to the Filter Design HDL Coder

The Filter Design HDL Coder generates hardware description language (HDL) code and test benches for filters you design with FDATool. The Filter Design HDL Coder accelerates the development of application-specific integrated circuit (ASIC) and field programmable gate array (FPGA) filter designs and bridges the gap between system-level design and hardware development by generating HDL code based on algorithms developed in MATLAB. Currently, system designers and hardware developers use HDLs, such as very high speed integrated circuit (VHSIC) hardware definition language (VHDL) and Verilog, to develop hardware designs. Although HDLs provide a proven method for hardware design, the task of coding filter designs and hardware designs in general, is labor intensive and the use of these languages for algorithm and system-level design is not optimal.

Using the Filter Design HDL Coder, system architects and designers can spend more time on fine-tuning algorithms and models through rapid prototyping and experimentation and less time on HDL coding. The architects and designers can efficiently design, analyze, simulate, and transfer system designs to hardware developers. In a typical use scenario, an architect or designer uses the Filter Design Toolbox, its Filter Design and Analysis Tool (FDATool), and the Filter Design HDL Coder to design and configure a filter. Then, with the click of a button, the Filter Design HDL Coder generates a VHDL or Verilog implementation of the design and specified test benches. The generated code adheres to a clean HDL coding style that enables architects and designers to quickly address customizations, as needed. The testbench feature increases confidence in the correctness of the generated code and saves potential time spent on testbench implementation.

The Filter Design HDL Coder features

- Graphical user interface (GUI) plug-in to the Filter Design and Analysis Tool (FDATool)
- MATLAB command line interface
- Support for the following filter structures:
 - Finite impulse response (FIR)
 - Antisymmetric FIR

- Transposed FIR
- Symmetric FIR
- Second-order section (SOS) infinite impulse response (IIR) Direct Form I
- SOS IIR Direct Form I transposed
- SOS IIR Direct Form II
- SOS IIR Direct Form II transposed
- Generation of code that adheres to a clean HDL coding style
- Options for controlling the contents and style of the generated HDL code
- Options for optimizing numeric results of generated HDL code
- Test bench generation for validating the generated HDL filter code
- Portable VHDL, portable Verilog, and ModelSim Tcl/Tk DO file test bench options

Known Software and Documentation Problems

This section includes a link to a description of known software and documentation problems in Version 1.0.

If you are viewing these Release Notes in PDF form, refer to the HTML form of the Release Notes, using either the Help browser or the MathWorks Web site and use the link provided.